Claim 1 recites that "the queue includes at least one dual-port random access memory (DPRAM) and wherein the number of banks corresponds to a number of address bits allocated in the DPRAM for one or more of the links, and wherein an address in the DPRAM is computed by combining a start address for one of the links and bits corresponding to an extra total address." The Colmant patent does not teach or suggest these features.

The Sakai publication discloses a DPRAM 51 which stores and outputs data received by a communication system. (See Figure 7). As disclosed in Paragraphs [38] and [85], the DPRAM rearranges frame data on a bit-by-bit basis for each frame. The Examiner relied on these portions of the Sakai publication to supply the features relating to the DPRAM recited in claim 1. However, there are differences.

Claim 1 recites a queue that includes at least one dual-port random access memory (DPRAM), and that "the number of banks corresponds to a number of address bits allocated in the DPRAM for one or more of the links" and that "an address in the DPRAM is computed by combining a start address for one of the links and bits corresponding to an extra total address." These features are not taught or suggested by Sakai. In Sakai, DPRAM 51 receives m-bit frame data. This data is then rearranged on a bit-by-bit basis.

In the Final Office Action, the Examiner compared the frames of Sakai to the banks of the claimed invention. However, these two are not the same. The frames of Sakai correspond to a frame (e.g., one or more packets) of received communication data. The communication data is received in frames and then stored on a bit-by-bit basis in DPRAM 51. The frames of Sakai,

therefore, define the size of the data received by the communication system, i.e., in packets or frames.

However, the banks of the claimed invention do not refer to the size of received data. Rather, the banks of claim 1 refer to the sections of the queue that are assigned to store data for a plurality of links. (See, for example, Figure 3). The DPRAM of Sakai has different data storage sections; however, Sakai does not teach or suggest that "the number of banks corresponds to a number of address bits allocated in the DPRAM for one or more of the links" and that "an address in the DPRAM is computed by combining a start address for one of the links and bits corresponding to an extra total address."

Without a teaching or suggestion of these features, it is respectfully submitted that claim 1 and its dependent claims are allowable.

Claim 6 recites that "the queue is formed from at least one dual-port random access memory (DPRAM) and wherein the number of banks corresponds to a number of address bits allocated in the DPRAM for one or more of the links." These features are not taught or suggested by the cited references, whether taken alone or in combination. Claim 7 recites similar features and therefore is allowable for similar reasons.

Dependent claim 8 recites that the banks are assigned by selecting a first link, checking whether the link is in use, and if the link is in use, checking whether a second link is in use and increasing a link count until a last link is checked; if the first link is not in use, assigning a desired number of banks to the first link and assigning a start address and an end address to the link; and assigning one or more banks to the second link by increasing a start address and end address of

the second link by referring to the end address of the first preceding link. These features are not taught or suggested by the cited references, whether taken alone or in combination.

Dependent claim 9 recites initializing address-related parameters of each link from a first link to a last link; if the initialization is completed through the last link, starting a read algorithm; checking whether there exists one item of data to be written in the queue beginning with the first link until the last link has been checked; and if there exists data to be written, writing the data using a write address and write enable signal and increasing a total address when the writing is completed; setting a write pointer with the increased total address, transmitting the write pointer to a signal detection unit and checking whether a current address of the link is the highest address of the bank by referring to the total address.

In addition, claim 9 recites that if the current address is the highest address, toggling write carry for the next link, assigning the lowest bits to the total address, or if the current address is not the highest address, checking whether there is data for the next link. These features are not taught or suggested by the cited references, whether taken alone or in combination.

Dependent claim 10 recites that the address-related parameters include a link start address, a link end address, a total address, and a write carry. These features are not taught or suggested by the cited references, whether taken alone or in combination.

Dependent claim 11 recites that when the current address of the link has not reached the highest address of the bank, if the restart condition arises, said flexible queue assignment method further comprises initializing address-related parameters of each link. These features are not taught or suggested by the cited references, whether taken alone or in combination.

Dependent claim 12 recites that generating the empty signal comprises determining a range of each link; from the first link to the last link, comparing the write carry and read carry sequentially and calculating a difference between write pointer and read pointer; and checking existence of data based on the difference of the pointers and generating the empty signal accordingly. These features are not taught or suggested by the cited references, whether taken alone or in combination.

Dependent claim 13 recites that range of each link indicates a number of banks assigned to each link and is determined by using a start address and an end address of each link. These features are not taught or suggested by the cited references, whether taken alone or in combination.

Dependent claim 14 recites determining a range of each link; from the first link to the last link, comparing the write carry and read carry sequentially and calculating a difference of pointers according to the comparison; and if the write carry and the read carry are the same, generating the full signal indicating a full or not-full state depending on whether said difference of pointers is within certain user-specified range. These features are not taught or suggested by the cited references, whether taken alone or in combination.

Dependent claim 15 recites that the difference of pointers is calculated by subtracting the read pointer from the write pointer if the write pointer and the read pointer are the same, or if the write pointer and the read pointer are not the same by calculating the difference of the write pointer and the read pointer reflecting the range of link. These features are not taught or suggested by the cited references, whether taken alone or in combination.

Dependent claim 16 recites checking whether the empty signal is in the not-empty state from the first link to the last link; if a link is detected to be in the not-empty state, reading data through read address and read enable signal connected to the queue; increasing read address and total address by the number of data items that have been read and checking whether the current address of the link is equal to the highest address of the bank; and if the current address of the link is equal to the highest address, toggling read carry and initializing total address with the lowest address of the bank, thereby moving to a next link. None of these features are taught or suggested by the cited references.

In view of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and timely allowance of the application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
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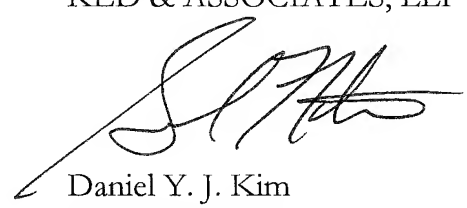

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